Amendments to the Claims:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

Listing of Claims:

Claim 1 (Currently Amended): A method of manufacturing a semiconductor package, comprising:

(a) providing a plurality of semiconductor chips and a wiring substrate, each of said plurality of semiconductor chips having an integrated circuit and bonding pads formed on a main surface thereof, said wiring substrate having a periphery and a first surface, a second surface opposed to said first surface and a plurality of conductive layers, said wiring substrate having a plurality of chip mounting areas at said first surface in a plane view, said plurality of chip mounting areas being arranged in a matrix formation of a rectangular shape having opposed longer sides and opposed shorter sides;

(b) mounting said plurality of semiconductor chips on said plurality of chip mounting areas of said first surface of said wiring substrate respectively;

(c) electrically connecting said bonding pads of said semiconductor chips with corresponding conductive layers of said plurality of conductive layers, by a plurality of bonding wires;

(d) sealing said plurality of semiconductor chips, said plurality of bonding wires and said first surface of said wiring substrate including said plurality of chip mounting areas by a resin member, said sealing being performed by a transfer molding such that said resin member is provided from one of the longer sides of the rectangular shape toward the other of the longer sides of the rectangular shape of

the matrix formation, via plural flow gates positioned at the periphery of the wiring substrate;

(e) forming a plurality of bump electrodes on said second surface of said wiring substrate so as to electrically connect with said plurality of conductive layers of said wiring substrate; and

(f) after (e), dividing said wiring substrate into plural parts each including a corresponding chip mounting area of said plurality of chip mounting areas, thereby to form a plurality of semiconductor packages each including one of said plural parts of said wiring substrate, one of said plurality of semiconductor chips, ones of said plurality of bonding wires and a part of said resin member.

Claim 2 (Original): A method of manufacturing a semiconductor package according to claim 1, wherein said wiring substrate includes a flexible tape substrate.

Claim 3 (Original): A method of manufacturing a semiconductor package according to claim 2, wherein said flexible tape substrate includes a polyimide tape.

Claim 4 (Original): A method of manufacturing a semiconductor package according to claim 2, wherein said flexible tape substrate includes a plurality of through holes passing through said flexible tape substrate in a thickness direction, wherein portions of said plurality of conductive layers are arranged to cover said plurality of through holes at said first surface of said wiring substrate, and wherein said plurality of bump electrodes are formed at said plurality of through holes so as to contact with said portions of said plurality of conductive layers.

Claim 5 (Original): A method of manufacturing a semiconductor package according to claim 4, wherein said plurality of bump electrodes are solder bump electrodes.

Claim 6 (Original): A method of manufacturing a semiconductor package according to claim 1, wherein (b) includes fixing each of said plurality of semiconductor chips on said first surface of said wiring substrate by an insulating adhesive layer respectively.

Claim 7 (Cancelled)

Claim 8 (New): A method of manufacturing a semiconductor package according to claim 1, wherein the matrix formation of the plurality of chip mounting areas includes groups of chip mounting areas clustered with each other, and the resin member is provided from one of the longer sides to a location among a respective group of chip mounting areas, and distributed from said location to each chip mounting area of said respective group of chip mounting areas.

Claim 9 (New): A method of manufacturing a semiconductor package according to claim 8, wherein each group of chip mounting areas includes four chip mounting areas, and wherein said location is among the four chip mounting areas.

Claim 10 (New): A method of manufacturing a semiconductor package according to claim 1, wherein said wiring substrate includes a plurality of wiring substrate members distributed along the direction of the longer sides of the

rectangular shape of the matrix formation, each wiring substrate member having a respective group of chip mounting areas clustered with each other.